Electronic Version

Stylesheet Version v1.1.1

Claims

[c1] 1. A MOSFET and a gate drive circuit adapted for very fast turn off for reduced crossover power losses, comprising a first MOSFET comprising a first MOSFET having a gate, a drain and a source for switching a load current equal to i_d; at least a second MOSFET having a gate, a drain and a source for turning off the first MOSFET; the source of the first MOSFET and the source of the at least a second MOSFET being connected together as a source connection; the gate of the first MOSFET and the drain of the at least a second MOSFET being connected together as a drain-gate connection; the gate of the first MOSFET being characterized by having a very low gate resistance; the on resistance of the at least a second MOSFET being characterized by having a very low channel resistance; the source connection being characterized by having a very low impedance; and the drain-gate connection being characterized by having a very low impedance, so that when the at least a second MOSFET is turned on, a gate current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET, and the gate current i_g is larger than the load current i_d.

[c2] 2. The MOSFET and gate drive circuit of claim 1 wherein the at least a second MOSFET is a large number of second MOSFETs; the source connection is a large number of source connections, and the drain-gate connection is a large number of drain-gate connections.

[c3] 3. The MOSFET and gate drive circuit of claim 2 wherein the large number of second MOSFETs are integrated into the first MOSFET die.

[c4] 4. The MOSFET and gate drive circuit of claim 2 wherein the first MOSFET comprises a first MOSFET die and the large number of second MOSFETs comprise a second MOSFET die, and the at least a second MOSFET die is immediately proximate to the first MOSFET die.

[c5] 5. The MOSFET and gate drive circuit of claim 4 wherein the second MOSFET die is mounted upon the first MOSFET die.

[c6] 6. The MOSFET and gate drive circuit of claim 2 wherein the large number of second MOSFETs are mounted upon the first MOSFET and connected thereto as a hybrid circuit.

[c7] 7. The MOSFET and gate drive circuit of claim 1 further comprising a local clamp circuit comprising a diode and

a capacitor immediate proximate to the first MOSFET.

[c8] 8. The MOSFET and gate drive circuit of claim 1 further comprising a gate turn on circuit comprising at least a third MOSFET connected to a source of voltage and an inductor connected to the at least a third MOSFET and to the gate of the first MOSFET.

[c9] 9. The MOSFET and gate drive circuit of claim 8 where the source of voltage is the drain of the first MOSFET.

[c10] 10. The MOSFET and gate drive circuit of claim 8 wherein the first MOSFET is one of a pair of MOSFETs in a push-pull circuit and the source of voltage is the drain of a second MOSFET of the pair of MOSFETs.

[c11] 11. The MOSFET and gate drive circuit of claim 9 further comprising a bilateral controlled rectifier connected be-tween the drain of the first MOSFET and the drain of the second MOSFET of the pair of MOSFETs.

[c12] 12. A method for turning off very quickly to reduce crossover power loss a first MOSFET that has a drain, a gate and a source and that is conducting a load current equal to i_d, the method comprising fabricating the first MOSFET so as to have a gate threshold cutoff voltage of V_{th} and a very low gate resistance, fabricating at least a second MOSFET having a drain, a gate and a source so

that the on resistance of the at least a second MOSFET is very low; connecting the source of the first MOSFET to the source of the at least a second MOSFET with a source to source connection having a very low resistance; connecting the gate of the first MOSFET to the drain of the at least a second MOSFET with a gate to drain connection having a very low resistance; such that the very low gate resistance if the first MOSFET plus the very low on resistance of the at least a second MOSFET plus the very low resistance of the source to source connection plus the very low resistance of the gate to drain connection is less than the ratio of V_{th} to I_d,turning on the at least a second MOSFET so that a current i_g will flow from the gate of the first MOSFET to the source of the first MOSFET through the at least a second MOSFET, and and the gate current i_g is larger than the load current i_d.

[c13] 13. A MOSFET and a gate drive circuit adapted for sequential turn off for reduced crossover power losses, comprising a first MOSFET comprising a first MOSFET having a gate, a drain and a source; a second MOSFET having a gate, a drain and a source, the source of the first MOSFET being connected to the source of the second MOSFETthe drain of the first MOSFET being connected to the drain of the second MOSFET; so that the first MOSFET and the second MOSFET are in parallel and

together switch a load current equal to i_d; the first MOSFET being larger than the second MOSFET, at least a third MOSFET having a gate, a drain and a source for turning off the first MOSFET; the gate of the first MOSFET and the drain of the at least a third MOSFET being connected together; the source of the first MOSFET and the source of the at least a third MOSFET being connected together; at least a fourth MOSFET having a gate, a drain and a source for turning off the second MOSFET; the gate of the second MOSFET and the drain of the at least a fourth MOSFET being connected together; the source of the second MOSFET and the source of the at least a fourth MOSFET being connected together; the gate of the first MOSFET being characterized by having a very low gate resistance; the on resistance of the at least a third MOSFET being characterized by having a very low channel resistance; the gate of the second MOSFET being characterized by having a very low gate resistance; the on resistance of the at least a fourth MOSFET being characterized by having a very low channel resistance; so that the third MOSFET may first be turned on so as to turn off the first MOSFET while the second MOSFET remains conducting to limit the rise of the voltage on the common drain connection of the first MOSFET and the second MOSFET so that the gate voltage of the first MOSFET is reduced to a low voltage with no significant Miller current; and the

fourth MOSFET may later be turned on so as to turn off the second MOSFET and interrupt the load current.